**axis\_readout\_v2**

Introduction

Compare to axis\_pfb\_readout\_v2, this ip can only demodulate a frequency at a time, but the max frequency it can demodulate could be much higher than that of axis\_pfb\_readout\_v2 limited only by the max sampling rate of ADC.

Specs

To know how to program values for the following quantities from python, see the section *qick python library*.

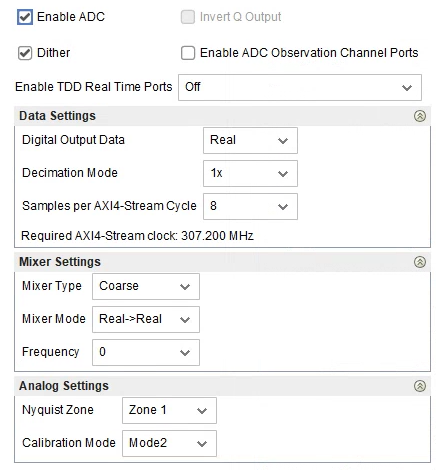
* DDS Frequency (fs is sampling rate of ADC): this is digital demodulation frequency. max input frequency is fs/2; min input frequencies is ?? (TODO: find min input freq). Actual min input frequency may be limited by external RF circuits (e.g. baluns).
* Power: input power range -5V ~ 2.1V (limited by ADC) [1].
* Waveform length: max waveform length is limited by axis\_avg\_buffer ip, which is also introduced in this thesis.

How to include it in firmware (zcu216, vivado2020.2)

IP core settings (double click on the ip):

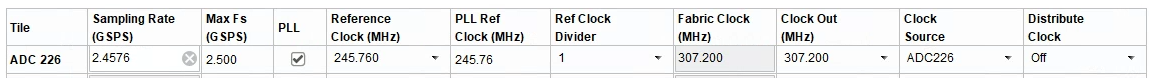
* “Fullspeed Output” checked

RFDC (Zynq Ultrascale+ RF Data Converter) DAC settings:

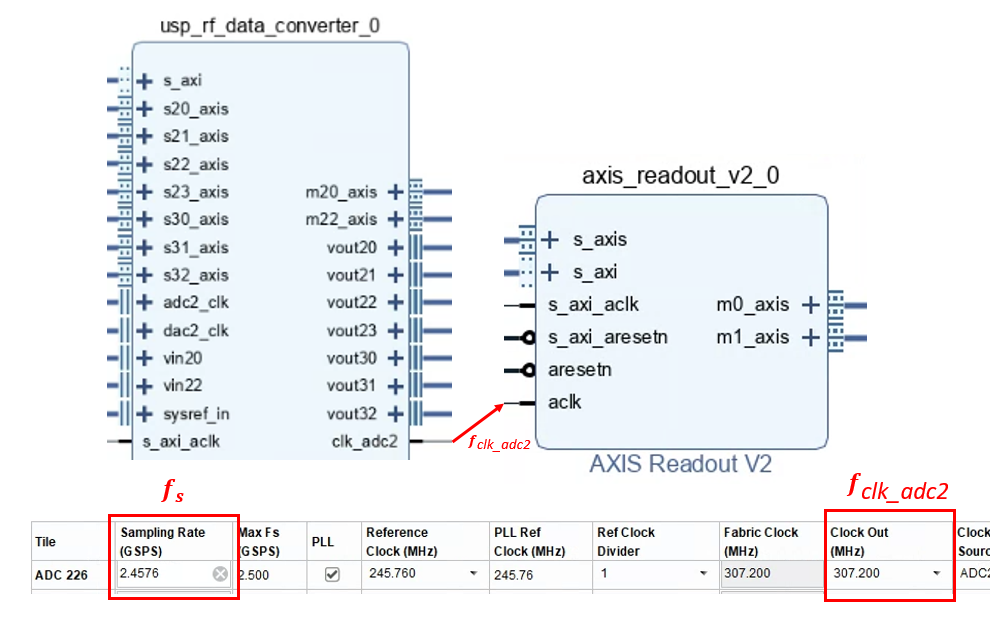


RFDC ADC tile clocking settings:

* For details about the fields see the section *rfdc settings*.
* For demo purposes, just select *Clock Source* to be the tile itself, and select *Distribution Clock* to be *off*. For details, see the section *rfdc settings*.



* Note that the relation between fs and faclk ( = fclk\_adc2 below) need to be fs = 8 \* faclk, where 8 is number of DDS inside the ip, which is not desinged to configurable. In this example, faclk = 307.2, fs = 2457.6 MHx, which satisfies the relation.

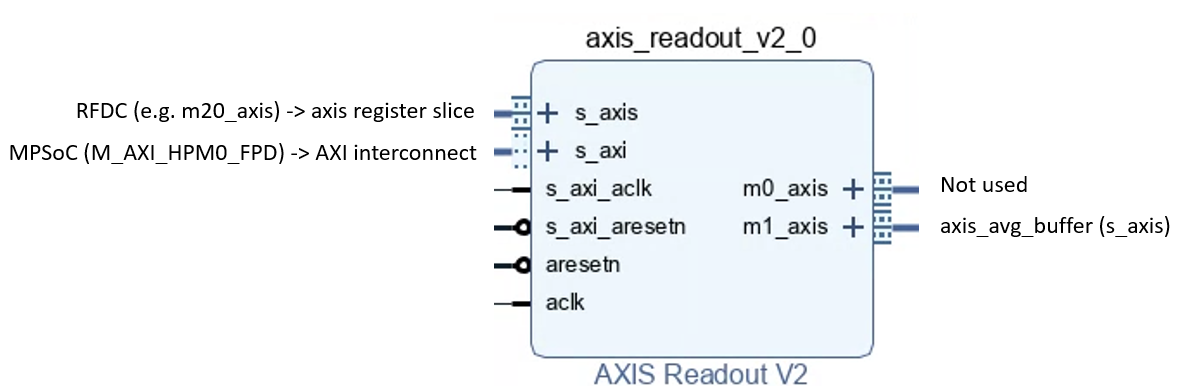


Wirings:

* For full details, you can re-create the vivado block design using the scripts (bd\_216 … .tcl, proj\_216 … .tcl) at:

<https://github.com/Ri-chard-Wu/thesis/tree/master/codes/full-speed-ro-sg-bd-scripts-216>

If you don’t know how to use the scripts, see the section *export & re-create vivado block design*.



References

[1] Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics (DS926).